AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application.

LISTING OF CLAIMS

1 – 11. Cancelled.

12. (previously presented) A method of communicating with a field programmable gate array (FPGA), comprising:

establishing an interface between a host computer and said FPGA;

transmitting configuration information over said interface in a first transmission mode to configure the FPGA to function according to a programmed configuration; and

transmitting operation information over said interface in a second transmission mode.

13. (Original) The method according to claim 12, wherein the programmed configuration comprises operation as a virtual device under test in an In-Circuit Emulation system.

14. (Original) The method according to claim 12, wherein the programmed configuration comprises operation as a virtual microcontroller in an In-Circuit Emulation system.

15. (previously presented) The method according to claim 12, wherein said interface comprises an IEEE 1284 compliant interface.

16. (previously presented) A method of communicating with a field programmable gate array (FPGA), comprising:

communicating an interface between a host computer and said FPGA to configure said FPGA to act as a virtual microcontroller;

executing instructions in synchronization on a microcontroller device and said virtual microcontroller; and

transmitting information between said host computer and said FPGA using said interface.

17. (previously presented) The method according to claim 16, wherein said interface comprises an IEEE 1284 compliant interface.

18. (previously presented) The method according to claim 16, wherein said FPGA is further configured to incorporate said interface.

19. (Original) A method of communication with a field programmable gate array (FPGA), comprising:

connecting a host computer to the FPGA using a communication interface;

programming a configuration into the FPGA, the configuration incorporating an implementation of the communication interface; and

carrying out non-programming communication between the host computer and the FPGA using the communication interface.

20. (Original) The method according to claim 19, wherein the communication interface comprises an IEEE 1284 compliant interface.

21. (Original) The method according to claim 19, wherein the configuration further incorporating a virtual microcontroller.

22. (Original) The method according to claim 21, wherein the virtual microcontroller executes instructions in synchronization with a microcontroller to carry out In-Circuit Emulation functions.

23. (previously presented) A method of communicating with an FPGA, comprising:

transmitting information over a parallel communication interface of an FPGA to configure the FPGA to act as a parallel port to receive data from a host computer system and to configure the FPGA to operate as a virtual microcontroller;

receiving data and communicating control information at said parallel port of said FPGA, the virtual microcontroller operating in lock step with a microcontroller under test; and

commanding the FPGA with instructions from the host computer system using the communication interface that configured the FPGA.

24. (Original) The method according to claim 23, wherein the parallel port comprises an IEEE 1284 compliant parallel port.

25. (Original) The method according to claim 23, wherein bidirectional IEEE 1284 compliant communication is carried out using extended parallel port (EPP) mode communication over the parallel port.

26. (Original) The method according to claim 23, further comprising conducting In-Circuit Emulation functions using the parallel port.